74HC573; 74HCT573

Octal D-type transparent latch; 3-state

Product data sheet

1. General description

The 74HC573; 74HCT573 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC573; 74HCT573 has octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state true outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all latches.

When LE is HIGH, data at the Dn inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The 74HC573; 74HCT573 is functionally identical to:

- 74HC563; 74HCT563, but inverted outputs
- 74HC373; 74HCT373, but different pin arrangement

2. Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors and microcomputers
- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to 74HC563; 74HCT563 and 74HC373; 74HCT373
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM EIA/JESD22-A114-C exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

PHILIPS

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
74HC573							
t_{PHL}, t_{PLH}	propagation delay	V_{CC} = 5 V; C_L = 15 pF					
	Dn to Qn			-	14	-	ns
	LE to Qn			-	15	-	ns
C_i	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance	per latch; V_I = GND to V_{CC}	[1]	-	26	-	pF
74HCT573							
t_{PHL}, t_{PLH}	propagation delay	V_{CC} = 5 V; C_L = 15 pF					
	Dn to Qn			-	17	-	ns
	LE to Qn			-	15	-	ns
C_i	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance	per latch; V_I = GND to (V_{CC} – 1.5 V)	[1]	-	26	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC573				
74HC573N	–40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HC573D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HC573DB	–40 °C to +125 °C	SSOP20	plastic small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HC573PW	–40 °C to +125 °C	TSSOP20	plastic small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HC573BQ	–40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

Table 2: Ordering information *…continued*

Type number	Package			
	Temperature range	Name	Description	Version
74HCT573				
74HCT573N	–40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HCT573D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT573DB	–40 °C to +125 °C	SSOP20	plastic small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HCT573PW	–40 °C to +125 °C	TSSOP20	plastic small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HCT573BQ	–40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

5. Functional diagram

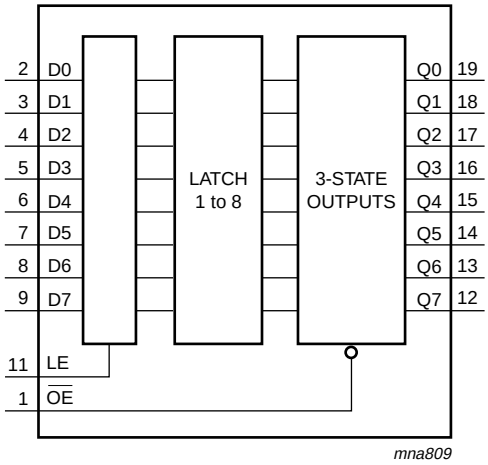


Fig 1. Functional diagram

Table 3: Pin description *...continued*

Symbol	Pin	Description
Q4	15	3-state latch output 4
Q3	16	3-state latch output 3
Q2	17	3-state latch output 2
Q1	18	3-state latch output 1
Q0	19	3-state latch output 0
V_{CC}	20	supply voltage

7. Functional description

Table 4: Function table [1]

Operating mode	Control		Input	Internal latches	Output
	$\overline{OE}$	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
			H	H	H
Latch and read register	L	L	l	L	L
			h	H	H
Latch register and disable outputs	H	L	l	L	Z
			h	H	Z

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
Z = high-impedance OFF-state.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = –0.5$ V to $(V_{CC} + 0.5$ V)	-	±35	mA
I_{CC}	quiescent supply current		-	70	mA
I_{GND}	ground current		-	–70	mA
T_{stg}	storage temperature		–65	+150	°C

Table 5: Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation					
	DIP20 package		[1]	-	750	mW
	SO20 package		[2]	-	500	mW
	SSOP20 package		[3]	-	500	mW
	TSSOP20 package		[3]	-	500	mW
	DHVQFN20 package		[4]	-	500	mW

[1] For DIP20 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO20 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP20 and TSSOP20 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C

[4] For DHVQFN20 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC573						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
t_r, t_f	input rise and fall time	V_{CC} = 2.0 V	-	-	1000	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	-	400	ns
74HCT573						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
t_r, t_f	input rise and fall time	V_{CC} = 4.5 V	-	6.0	500	ns

Table 7: Static characteristics 74HC573 *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 7.8 mA; V_{CC} = 6 V	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6 V	-	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	-	-	±5.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	µA
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = −20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = −6.0 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = −7.8 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	-	-	±10.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	160	µA

Table 8: Static characteristics 74HCT573

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V

Table 8: Static characteristics 74HCT573 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = –20 µA	4.4	4.5	-	V
		I_O = –6.0 mA	3.98	4.32	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 µA	-	0	0.1	V
		I_O = 6.0 mA	-	0.16	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND per input pin; other inputs at GND or V_{CC}; I_O = 0 A; V_{CC} = 5.5 V	-	-	±0.5	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	µA
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V				
	Dn		-	35	126	µA
	LE		-	65	234	µA
	$\overline{OE}$		-	125	450	µA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = –20 µA	4.4	-	-	V
		I_O = –6.0 mA	3.84	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 µA	-	-	0.1	V
		I_O = 6.0 mA	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND per input pin; other inputs at GND or V_{CC}; I_O = 0 A; V_{CC} = 5.5 V			±5.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	80	µA
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V				
	Dn		-	-	158	µA
	LE		-	-	293	µA
	$\overline{OE}$		-	-	563	µA

Table 8: Static characteristics 74HCT573 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = −20 μA	4.4	-	-	V
		I_O = −6.0 mA	3.7	-	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 μA	-	-	0.1	V
		I_O = 6.0 mA	-	-	0.4	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±1.0	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND per input pin; other inputs at GND or V_{CC}; I_O = 0 A; V_{CC} = 5.5 V	-	-	±10.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	160	μA
ΔI_{CC}	additional quiescent supply current	per input pin; V_I = V_{CC} − 2.1 V; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V				
	Dn		-	-	172	μA
	LE		-	-	319	μA
	$\overline{OE}$		-	-	613	μA

11. Dynamic characteristics

Table 9: Dynamic characteristics 74HC573

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t_{PHL}, t_{PLH}	propagation delay Dn to Qn	see Figure 7				
		V_{CC} = 2.0 V	-	47	150	ns
		V_{CC} = 4.5 V	-	17	30	ns
		V_{CC} = 5 V; C_L = 15 pF	-	14	-	ns
		V_{CC} = 6.0 V	-	14	26	ns
t_{PHL}, t_{PLH}	propagation delay LE to Qn	see Figure 8				
		V_{CC} = 2.0 V	-	50	150	ns
		V_{CC} = 4.5 V	-	18	30	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	ns
		V_{CC} = 6.0 V	-	14	26	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	see Figure 9				
		V_{CC} = 2.0 V	-	44	140	ns
		V_{CC} = 4.5 V	-	16	28	ns
		V_{CC} = 6.0 V	-	13	24	ns

Table 9: Dynamic characteristics 74HC573 *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_W	pulse width LE HIGH	see Figure 8				
		V_{CC} = 2.0 V	120	-	-	ns
		V_{CC} = 4.5 V	24	-	-	ns
		V_{CC} = 6.0 V	20	-	-	ns
t_{su}	set-up time Dn to LE	see Figure 10				
		V_{CC} = 2.0 V	75	-	-	ns
		V_{CC} = 4.5 V	15	-	-	ns
		V_{CC} = 6.0 V	13	-	-	ns
t_h	hold time Dn to LE	see Figure 10				
		V_{CC} = 2.0 V	5	-	-	ns
		V_{CC} = 4.5 V	5	-	-	ns
		V_{CC} = 6.0 V	5	-	-	ns

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Table 10: Dynamic characteristics 74HCT573

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
t_{PHL}, t_{PLH}	propagation delay Dn to Qn	see Figure 7					
		V_{CC} = 4.5 V		-	20	35	ns
		V_{CC} = 5 V; C_L = 15 pF		-	17	-	ns
t_{PHL}, t_{PLH}	propagation delay LE to Qn	see Figure 8					
		V_{CC} = 4.5 V		-	18	35	ns
		V_{CC} = 5 V; C_L = 15 pF		-	15	-	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	V_{CC} = 4.5 V; see Figure 9		-	17	30	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn	V_{CC} = 4.5 V; see Figure 9		-	18	30	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V; see Figure 7		-	5	12	ns
t_W	pulse width LE HIGH	V_{CC} = 4.5 V; see Figure 8		16	5	-	ns
t_{su}	set-up time Dn to LE	V_{CC} = 4.5 V; see Figure 10		13	7	-	ns
t_h	hold time Dn to LE	V_{CC} = 4.5 V; see Figure 10		9	4	-	ns
C_{PD}	power dissipation capacitance	per latch; V_I = GND to (V_{CC} – 1.5 V)	[1]	-	26	-	pF

Table 10: Dynamic characteristics 74HCT573 *...continued*

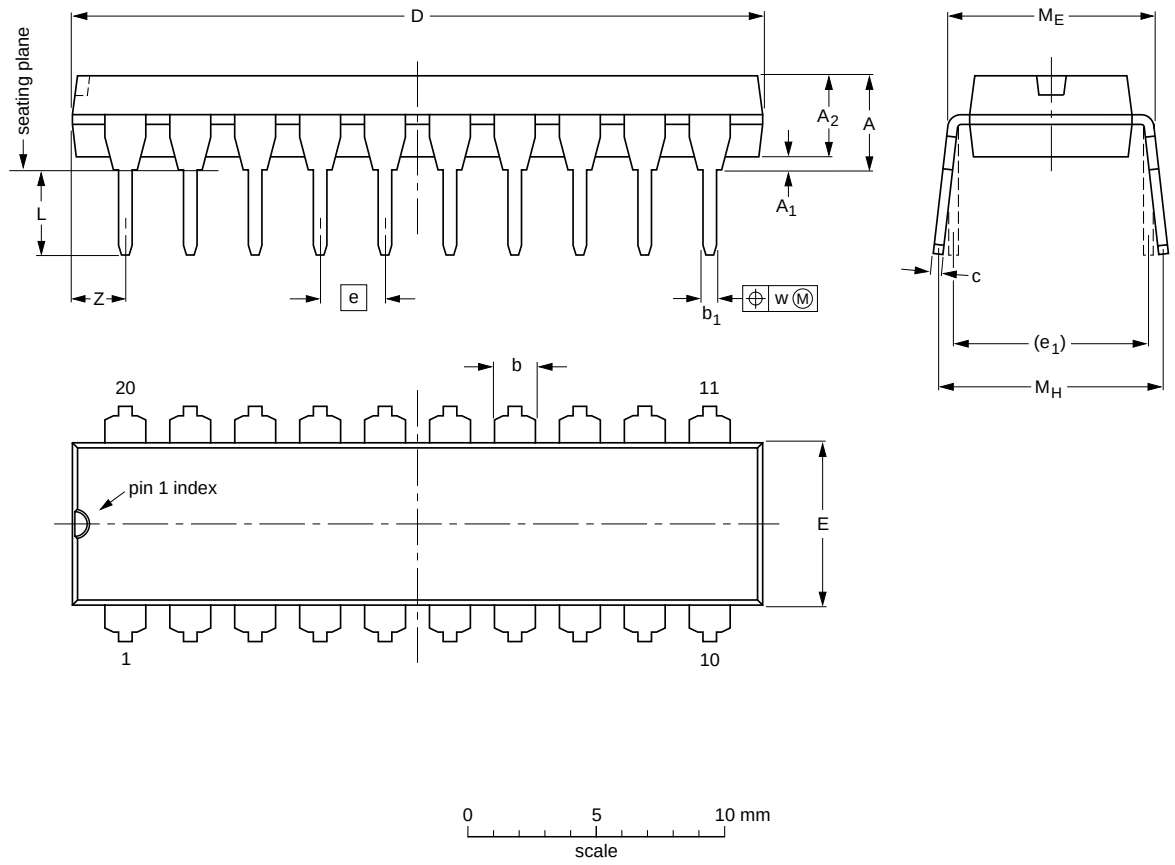
Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 to +85 °C						
t_{PHL}, t_{PLH}	propagation delay Dn to Qn	V_{CC} = 4.5 V; see Figure 7	-	-	44	ns
t_{PHL}, t_{PLH}	propagation delay LE to Qn	V_{CC} = 4.5 V; see Figure 8	-	-	44	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	V_{CC} = 4.5 V; see Figure 9	-	-	38	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn	V_{CC} = 4.5 V; see Figure 9	-	-	38	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V; see Figure 7	-	-	15	ns
t_W	pulse width LE HIGH	V_{CC} = 4.5 V; see Figure 8	20	-	-	ns
t_{su}	set-up time Dn to LE	V_{CC} = 4.5 V; see Figure 10	16	-	-	ns
t_h	hold time Dn to LE	V_{CC} = 4.5 V; see Figure 10	11	-	-	ns
T_{amb} = −40 to +125 °C						
t_{PHL}, t_{PLH}	propagation delay Dn to Qn	V_{CC} = 4.5 V; see Figure 7	-	-	53	ns
t_{PHL}, t_{PLH}	propagation delay LE to Qn	V_{CC} = 4.5 V; see Figure 8	-	-	53	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	V_{CC} = 4.5 V; see Figure 9	-	-	45	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn	V_{CC} = 4.5 V; see Figure 9	-	-	45	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V; see Figure 7	-	-	18	ns
t_W	pulse width LE HIGH	V_{CC} = 4.5 V; see Figure 8	24	-	-	ns
t_{su}	set-up time Dn to LE	V_{CC} = 4.5 V; see Figure 10	20	-	-	ns
t_h	hold time Dn to LE	V_{CC} = 4.5 V; see Figure 10	14	-	-	ns

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

13. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			

Fig 12. Package outline SOT146-1 (DIP20)